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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,410	12/29/2000	Mark Owen Homewood	00-BN-056 (STMI01-00056)	7823

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	4

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,410	HOMEWOOD ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Emma et al., US Patent 4,991,080.

4. Referring to claim 1, Emma et al. have taught a data processor having a clustered architecture comprising:

a. a branching cluster (Figure 3, elements 301 and 501) and a non-branching cluster (Figure 3, elements 701, 201, 401, 601), each capable of computing branch conditions (Column 16, lines 40-55, column 23, lines 37-47, column 22, lines 39-59, column 23, lines 24-30), said branching cluster operable to perform branch address computations for said branching cluster and said non-branching cluster (Column 16, lines 40-55, column 23, lines 37-47); and

b. remote conditional branching control circuitry that causes said branching cluster to perform a branch address computation in response to sensing a conditional branch instruction in said non-branching cluster (column 22, lines 39-59, column 23, lines 24-

30), and that communicates a computed branch condition from said non-branching cluster to said branching cluster (Figure 3, element 581).

5. Referring to claim 2, Emma et al. have taught the data processor as set forth in claim 1 wherein each of said branching cluster (Figure 13, element 565 and 547) and said non-branching cluster (Figure 16, element 723) comprises at least one register file.

6. Referring to claim 3, Emma et al. have taught the data processor as set forth in claim 1, as described above, and wherein each of said branching cluster (column 17, lines 43-46) and said non-branching cluster (column 10, lines 22-27) comprises an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing at least one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline (column 10, lines 22-27, column 17, lines 43-46).

7. Referring to claim 4, Emma et al. have taught the data processor as set forth in claim 1, as described above, and wherein said remote conditional branching control circuitry further causes said branching cluster to perform a next program counter address computation in response to sensing a conditional branch instruction in said non-branching cluster (abstract, column 22, lines 39-59, column 23, lines 24-30).

8. Referring to claim 5, Emma et al. have taught the data processor as set forth in claim 4, as described above, and wherein said remote conditional branching control circuitry selects one of said computed next program counter address and said computed branch address in response to said computed branch condition (Column 22, lines 39-59, column 23, lines 24-30, Figure 6, elements 209 and 219).

9. Referring to claim 6, Emma et al. have taught the data processor as set forth in claim 5, as described above, and wherein said remote conditional branching control circuitry comprises a multiplexor that is responsive to said computed branch condition (Figure 6, elements 209 and 219).

10. Referring to claim 7, Emma et al. have taught the data processor as set forth in claim 1 wherein said data processor issues a shadow conditional branch instruction in said branching cluster to perform said branch address computation in response to sensing said conditional branch instruction in said non-branching cluster (Column 17, lines 18-46, Every instruction the branch coprocessor executes is a shadow conditional branch instruction.).

11. Claim 8 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

12. Referring to claim 9, Emma et al. have taught the method of operating said data processor as set forth in claim 8 further comprising the step of computing said branch condition in said non-branching cluster (column 22, lines 39-59, column 23, lines 24-30).

13. Referring to claim 10, Emma et al. have taught the method of operating said data processor as set forth in claim 9 further comprising the step of computing a next program counter address (abstract, column 16, lines 40-55).

14. Claim 11 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

15. Claim 12 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

16. Claim 13 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al., US Patent 4,991,080, in view of Boettner et al., US Patent 4,777,589.

19. Referring to claim 14, Emma et al. have taught a processing system comprising:

a. a data processor having a clustered architecture (Figure 3);

b. a memory associated with said data processor (Figure 3, element 101);

c. wherein said data processor comprises:

i. at least a branching cluster (Figure 3, elements 301 and 501) and a non-branching cluster (Figure 3, elements 701, 201, 401, 601) that are capable of computing branch conditions (Column 16, lines 40-55, column 23, lines 37-47, column 22, lines 39-59, column 23, lines 24-30), said branching cluster operable to perform branch address computations for said at least said branching cluster and said non-branching cluster (Column 16, lines 40-55, column 23, lines 37-47);

ii. and remote conditional branching control circuitry that causes said branching cluster to perform a branch address computation in response to sensing

a conditional branch instruction in said non-branching cluster (column 22, lines 39-59, column 23, lines 24-30), and that communicates a computed branch condition from said non-branching cluster to said branching cluster (Figure 3, element 581).

20. Emma et al. have not taught a plurality of peripheral circuits associated with said data processor for performing selected functions in association with said data processor. Boettner et al. have taught a plurality of peripheral circuits for performing selected functions in association with said data processor (Boettner et al. column 1, lines 22-39) in order to process I/O devices by procedures implemented in a higher level language. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Emma et al. include the plurality of peripheral circuits for performing selected functions in association with said data processor, as taught by Boettner et al., for the desirable purpose of accessing I/O devices by procedures implemente din a higher level language. (Boettner et al., column 1,lines 22-39)

21. Claim 15 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

22. Claim 16 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

23. Claim 17 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

24. Claim 18 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

25. Referring to claim 19, Emma et al. have taught the processing system as set forth in claim 18 wherein said remote conditional branching control circuitry comprises a multiplexor having an input channel associated with said non-branching cluster, said multiplexor responsive to said computed branch condition (Figure 6, elements 209 and 219).

26. Claim 20 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER